In the Claims

Please cancel claims 17-25, 38, 40, and 47-50. Amend claims 39, 41, 42, 43, 45, and 46. Add new claim 51. The claims are as follows:

1. – 38. (CANCELLED)

39. (CURRENTLY AMENDED) The method of fabricating a shadow mask as recited in claim ~~38~~ 41, wherein said improved contact processing of said perimeter chips is additional dummy solder bumps to support a second shadow mask ~~used to deposit an additional layer of material on said solder bumps so said second shadow mask does not damage perimeter chip solder bumps~~.

40. (CANCELLED)

41. (CURRENTLY AMENDED) ~~The method of fabricating a shadow mask as recited in claim 40,~~

A method of fabricating a shadow mask, comprising the steps of:

a) providing an array of holes in the shadow mask corresponding to contacts on an array of chips on a wafer, said array of chips including perimeter chips extending along a periphery of the wafer; and

b) providing additional dummy holes in the shadow mask located adjacent holes corresponding to most of said perimeter chips wherein said additional dummy holes are for improving contact processing of said perimeter chips wherein said additional dummy holes are omitted in saw blade lanes and in a ring shaped exclusion zone ~~along said periphery~~ in an area of the shadow mask beyond said perimeter chips and beyond said dummy holes.

42. (CURRENTLY AMENDED) The method of fabricating a shadow mask as recited in claim 41 ~~40~~, further comprising the step of inspecting the shadow mask using dummy holes along an edge of a dicing lane to align the shadow mask to an inspection device.

43. (CURRENTLY AMENDED) The method of fabricating a shadow mask as recited in claim 41 ~~40~~, further comprising the step of inspecting the shadow mask using a pattern of additional holes, said additional holes located beyond holes corresponding to said perimeter chips, said additional holes for aligning the shadow mask to an inspection device, wherein said pattern of additional holes does not print on the wafer.

44. (ORIGINAL) The method of fabricating a shadow mask as recited in claim 43, wherein said pattern of additional holes is located so that it will be covered by a guard ring.

45. (CURRENTLY AMENDED) The method of fabricating a shadow mask as recited in claim ~~40~~, further comprising the step of inspecting the shadow mask using a covering for said additional dummy holes.

46. (CURRENTLY AMENDED) The method of fabricating a shadow mask as recited in claim 41 ~~40~~, wherein said covering for said additional dummy holes is a ring having an inside edge corresponding to outside edges of perimeter chips.

47. – 50. (CANCELLED).

51. (NEW) A method of fabricating a shadow mask, comprising the steps of:

a) providing an array of holes in the shadow mask corresponding to contacts on an array of chips on a wafer, said array of chips including perimeter chips extending along a periphery of the wafer; and

b) providing additional dummy holes in the shadow mask located adjacent holes corresponding to most of said perimeter chips wherein said additional dummy holes are for improving contact processing of said perimeter chips wherein said additional dummy holes are omitted in a ring shaped exclusion zone in an area of the shadow mask beyond said perimeter chips and beyond said dummy holes.